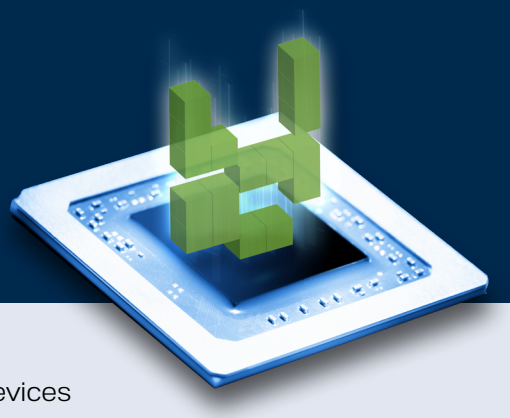
slate

TTTech industrial

Edge IP Solution

2+1/4+1 Port TSN Switched Endpoint IP and Software for FPGA



- Fast, easy integration into planned and existing FPGA-based devices
- Provides guaranteed low-latency communication for critical traffic
- Reference designs available for Intel evaluation platforms
- Seamless compatibility with TTTech Industrial Slate network planning software

Edge IP Solution offers highly configurable TSN functionality for industrial devices. Edge IP Solution includes IP core and associated software stacks for fast and easy integration onto your FPGA – enabling open, standard deterministic switching functionality. Edge IP Solution is available for Intel Cyclone V (SoC), Cyclone 10 GX and Arria 10 (SoC) FPGAs.

TSN Switching

Standards Support
Edge IP Solution supports the core TSN mechanisms of time-synchronization (IEEE 802.1AS-2020) and time aware shaping (IEEE 802.1Qbv) as well as other mechanisms such as frame preemption (IEEE 802.1Qbu), seamless redundancy (IEEE 802.1CB) and cut-through.

Network Configuration
Edge IP Solution includes a NETCONF stack and the YANG models required to make TSN devices configurable. Edge IP Solution combines with TTTech Industrial Slate network planning software to make building topologies, adding streams and deploying configurations for TSN networks easy.

Ease of Integration

Configurable Design Block
The Edge IP Solution Qsys component enables users to choose from a range of xMII interfaces and other system parameters. IP features can be adapted to find the right balance between size and functionality, resulting in an optimal footprint for your application. Interconnect logic between IP functions and subsystems can be automatically generated to save time and effort in FPGA design.

Reference Design
An Edge IP Solution reference design is available Intel FPGAs. The Cyclone V (SoC)-based TTTech Industrial Evaluation Board can be used as a stand-alone 4+1 port switched endpoint when designing and building TSN products with Edge IP Solution.

Contact us at
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www.tttech-industrial.com

Product Features

Ports	2+1/4+1 ports; 10/100/1000 Mbit/s
Target Devices	Intel Cyclone V (SoC), Intel Arria 10 (SoC)
Physical Interfaces	MII, GMII, DMA for host PPS (Pulse-Per-Second) output Avalon slave interface for management register access
Reference Designs	TTTech Industrial Evaluation Board (Intel Cyclone V SoC) Intel Arria 10 SoC Development Kit
Supported Ethernet Interfaces	MII, GMII, RMII, RGMII, SGMII, 100BASE-FX, 1000BASE-X
TSN	IEEE 802.1AS-2020 Time Synchronization IEEE 802.1Qbv Time Aware Shaping IEEE 802.1Qbu Frame Preemption IEEE 802.1CB Frame Replication and Elimination for Reliability
IEEE 802.1Q	Port-based VLAN classification Assignment to traffic class on ingress ports Support for credit-based shaper (CBS)
Clock Synchronization	IEEE 802.1AS-2020 (multi-time domain support) IEEE 1588-2019 one-step end-to-end transparent clock support
Configuration	NETCONF 1.0/1.1 (RFC 6241) including derived YANG models – IEEE 802.1Qbv Time Aware Shaping – IEEE 802.1Qbu Frame Preemption – IEEE 802.1Qcp Bridges and Bridged Networks (VLAN support) SNMP v1/v2/v3 (RFC 3416) including MIB
Switching Engine	Store and forward architecture providing full cross-sectional bandwidth 128-512 kbit frame buffer per port 4096 VLANs, up to 64 MSTIs 16 MAC address filters per port Up to 4096 entry MAC address hash-based learning table Up to 4096 policers per port 8 traffic shapers per port (optional) Static configuration of MAC addresses Flow identification-based MAC addresses Ingress rate-limiting on a per-port basis for unicast, multicast, and broadcast traffic
Operating System	Linux kernel 5.4 LTS Support for Linux net_dev, switch_dev, and PHC (PTP hardware clock)
Embedded Software	Linux kernel module Native Linux interfaces / user space configuration library Edge PTP in binary format for ARM – for IEEE 1588 / IEEE 802.1AS clock synchronization MSTP including additions for engineered traffic (802.1Qcc) Open source support for SNMP and NETCONF
Delivery	Encrypted Qsys IP component including interface adapters to xMII Software and device drivers for Linux YOCTO based build system Ready-made boot image Reference design for the DE-Evaluation Board Edge and the Intel Arria 10 (SoC) Development Kit MIBs and YANG models Getting started guide Technical documentation

Material name	Material number
DE-IP Solution Edge License Seat	12643
DE-IP Solution Edge License Float	13234
DE-IP Solution Edge Royalty	12647

Material name	Material number
DE-IP Solution Edge ACM	13709
DE-IP Solution Edge 8 Port Ext	13487

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