slate

TTTech industrial

Flex IP Solution

Flexible Deterministic Ethernet IP Core with TSN (Time Sensitive Networking)

- Configurable and scalable features for optimal silicon design-in
- Delivered according to ASIC development requirements
- Provides guaranteed low-latency communication for critical traffic
- Includes Linux software reference for switch and switched-endpoint operation

Flex IP Solution is a flexible design IP for customized chip or ASIC products. Flex IP Solution offers a wide range of configurable features and a verification environment that enables developers to check the coverage and quality of IP. Flex IP Solution source code is developed and delivered according to ASIC requirements e.g. memories instantiated on top-level.

TSN Switch Features

IEEE 802.1AS Time Synchronization
Profile of IEEE 1588v2 for synchronization of clocks in the network. Supports timing requirements for scheduled TSN networks.

IEEE 802.1Qcc SRP Enhancements
Defines the interfaces for central configuration of TSN networks. Supports configuration models for dynamic scheduling of TSN.

IEEE 802.1CB Seamless Redundancy
Enables seamless redundancy for increased network availability. Allows for redundancy on a per stream basis for individual critical streams.

IEEE 802.1Qbv Time Aware Shaping
Provides guaranteed communication latency for time-critical traffic over standard Ethernet even in a converged infrastructure.

IEEE 802.1Qbu Frame Preemption
Allows for optimal bandwidth utilization of non-scheduled background traffic sent in parallel with scheduled traffic.

IEEE 802.1Qci Filtering and Policing
Protects against faulty and/or malicious endpoints and switches. Isolates faults to specific regions in the network. (Available 2021)

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Product Features

Ports	3 to 12 ports; 10/100/1000 Mbit/s
Physical Interfaces	MII, GMII, DMA for host PPS (Pulse-Per-Second) output AXI, Avalon or AHB slave interface for management register access AXI or Avalon master interface for DMA to host CPU
Supported Ethernet Interfaces	MII, GMII, RMII, RGMII, SGMII, 100BASE-FX, 1000BASE-X
TSN	IEEE 802.1AS-2020 Time Synchronization IEEE 802.1Qbv Time Aware Shaping IEEE 802.1Qcc SRP Enhancements IEEE 802.1Qbu Frame Preemption IEEE 802.1CB Frame Replication and Elimination IEEE 802.1Qci Filtering and Policing (Available 2021)
AVB	IEEE 802.1AS-2020 Time Synchronization for Time-Sensitive Applications (gPTP) IEEE 802.1Qav Forwarding and Queuing for Time-Sensitive Streams (FQTSS)
HSR	HSR RedBox, HSR End Node, HSR-PRP RedBox and QuadBox support
PRP	PRP RedBox and DANP support
IEEE 802.1Q	Port-based VLANs and VLAN tagging Prioritization of packets on egress ports Untagging of VLAN frames on egress ports
Clock Synchronization	IEEE 802.1AS-2020 (including multi-time domain support) IEEE 1588-2019 one-step end-to-end transparent clock support
Switching Engine	Store and forward architecture providing full cross-sectional bandwidth 128-512 kbit frame buffer per port 4096 VLANs, up to 64 MSTIs 16 MAC address filters per port Up to 4096 entry MAC address hash-based learning table Up to 4096 policer per port 8 traffic shapers per port (optional) Static configuration of MAC addresses Flow identification-based MAC addresses Ingress rate-limiting on a per-port basis for unicast, multicast, and broadcast traffic
Embedded Software	Linux kernel module Native Linux interfaces / user space configuration library Edge PTP in binary format for ARM – for IEEE 1588 / IEEE 802.1AS clock synchronization MSTP including additions for engineered traffic (IEEE 802.1Qcc) Open source support for SNMP and NETCONF
Delivery	IP core design files in source code Software and device drivers for Linux YOCTO based build system Integration manual Verification environment Test report Technical documentation

Material name	Material number
DE-IP Solution Flex License	12642

Material name	Material number
DE-IP Solution Flex Royalty	12644

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