Edge IP Solution

3/5-Port Deterministic Ethernet IP Solution with TSN (Time Sensitive Networking)

- Fast, easy integration into planned and existing FPGA-based devices
- Provides guaranteed low-latency communication for critical traffic
- Includes the latest IEEE 802.1 Ethernet standards
- Seamless compatibility with TTTech Industrial Slate XNS network planner and topology builder

TTTech Industrial's Edge IP Solution is the simple way to add TSN (Time Sensitive Networking) Ethernet functionality to switched endpoint devices such as industrial controllers. Edge IP Solution includes IP core and associated software for fast and easy integration onto your FPGA enabling open, standard deterministic switching functionality.

**TSN Switching**

**Standards Support**
Edge IP Solution supports the core TSN mechanisms of time-synchronization (IEEE 802.1AS) and time aware shaping (IEEE 802.1Qbv) as well as other mechanisms such as frame preemption (IEEE 802.1Qbu) and cut-through.

**Network Configuration**
Edge IP Solution combines with TTTech Industrial Slate XNS software to make building topologies, adding streams and deploying configurations for TSN networks easy. TTTech Industrial's high-performance planning engine is built in to the Slate XNS software for planning IEEE 802.1Qbv and 802.1Qbu traffic as well as cut-through data streams.

**Ease of Integration**

**Configurable Design Block**
The Edge IP Solution Qsys component enables users to choose from a range of xMII interfaces and other system parameters. IP features can be adapted to find the right balance between size and functionality, resulting in an optimal footprint for your application. Interconnect logic between IP functions and subsystems can be automatically generated to save time and effort in FPGA design.

**Evaluation**
An Edge IP Solution reference design is available for the TTTech Industrial Evaluation Board for use as a stand-alone 4-port switched endpoint device. Combined with Slate XNS, this provides a comprehensive package for designing and building TSN evaluation systems.

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## Ports
- 3 to 5 ports; 10/100/1000 Mbit/s

## Target Devices
- Intel Cyclone V (SoC), Intel Arria 10 (SoC)

## Physical Interfaces
- MII, GMII, DMA for host
- PPS (Pulse-Per-Second) output
- Avalon slave interface for management register access

## Reference Designs
- TTTech Industrial Evaluation Board (Intel Cyclone V SoC)
- Intel Arria 10 SoC Development Kit

## Supported Ethernet Interfaces
- MII, GMII, RMII, RGMII, SGMII,
- 100BASE-FX, 1000BASE-X

## TSN
- IEEE 802.1AS-2020 Time Synchronization
- IEEE 802.1Qbv Time Aware Shaping
- IEEE 802.1Qbu Frame Preemption
- IEEE 802.1ICB Frame Replication and Elimination for Reliability

## IEEE 802.1Q
- Port-based VLAN classification
- Assignment to traffic class on ingress ports
- Support for credit-based shaper (CBS)

## Clock Synchronization
- IEEE 802.1AS-2020 (multi-time domain support)
- IEEE 1588-2019 one-step end-to-end transparent clock support

## Configuration
- NETCONF 1.0/1.1 (RFC 6241) including derived YANG models
  - IEEE 802.1Qbv Time Aware Shaping
  - IEEE 802.1Qbu Frame Preemption
  - IEEE 802.1Qcp Bridges and Bridged Networks (VLAN support)
- SNMP v1/v2/v3 (RFC 3416) including MiB

## Switching Engine
- Store and forward architecture providing full cross-sectional bandwidth
  - 128–512 kbit frame buffer per port
  - 4096 VLANs, up to 64 MSTIs
  - 16 MAC address filters per port
  - Up to 4096 entry MAC address hash-based learning table
  - Up to 4096 policers per port
  - 8 traffic shapers per port (optional)
  - Static configuration of MAC addresses
  - Flow identification-based MAC addresses
  - Ingress rate-limiting on a per-port basis for unicast, multicast, and broadcast traffic

## Operating System
- Linux Kernel 4.14 LTS (optional real-time patch)
- Support for Linux net_dev, switch_dev, and PHC (PTP hardware clock)

## Embedded Software
- Linux kernel module
- Native Linux interfaces / user space configuration library
- Edge PTP in binary format for ARM – for IEEE 1588 / IEEE 802.1AS clock synchronization
- MSTP including additions for engineered traffic (802.1Qcc)
- Open source support for SNMP and NETCONF

## Delivery
- Encrypted Qsys IP component including interface adapters to xMII
- Software and device drivers for Linux
- YOCTO based build system
- Ready-made boot image
- Reference design for the DE-Evaluation Board Edge
- MiBs and YANG models
- Getting started guide
- Technical documentation

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**Material Features**

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